CALIBRATION CONFIGURATION

Background of the Invention:

Field of the Invention:

The present invention relates to a calibration configuration for setting an adjustable impedance.

Calibration of an integrated circuit requires the presence of a precisely defined reference resistor, relative to which the circuit can be calibrated.

To determine the system characteristics of a circuit configuration, it is necessary to specify the output impedance in order to determine reliable values with regard to time behavior of the signal outputting, voltage consumption, and current consumption. Fluctuations with regard to the output impedance cannot be defined exactly on account of process fluctuations, operating temperature of the semiconductor chip, etc. Various calibration methods are employed nowadays in order to set specific electrical quantities to a desired amount and to eliminate manipulated variables that change during operation. A preferred method is, for example, the calibration of a circuit configuration for setting a desired output impedance relative to a reference resistor.

Electronik-Grundlagen [Principles of electronics], 9th edition, Verlag Europa-Lehrmittel, Europa-No.: 31789, page 298, shows a circuit configuration corresponding to FIG. 1 having two resistors R1 and R2, which are connected in series in a first current path, and having two resistors R3 and R4, which are connected in series in a second current path. The positive supply potential VDDQ and the negative supply potential VSSQ of a supply voltage are fed to the ends of the current paths. The resistor R3 illustrated in the second current path is a resistor that is to be calibrated and can be set with regard to its resistance or impedance. Between the current paths, which also represent voltage dividers, a voltmeter is located in the actual bridge path. If the voltages U1 and U3 and, respectively, U2 and U4 across the resistors R1, R2, R3, and R4 are of the same magnitude, the null indicator exhibits no deflection. The bridge is balanced. Because the resistors are proportional to the voltages, the variable resistor can be determined by a ratio calculation:

$$U1/U2 = U3/U4.$$

This also leads to the relationship: $R1/R2 = R3/R4$.

Consequently, the resistor R3 can be derived:

$$R3 = R4 \times (R1/R2).$$

The circuit configuration illustrated is also referred to as a resistance measuring bridge for measuring an electrical resistance by current or voltage comparison of the resistor to be measured and of the known resistors.

With the use of a reference resistor for calibrating an output impedance of a circuit configuration, the two configurations described below are predominantly provided in a circuit configuration.

One possibility is, for example, the use of an off-chip reference resistor - not situated within the semiconductor chip - relative to which the circuit configuration is calibrated. Such a method has the advantage that the reference resistor situated externally with respect to the semiconductor chip can be set very precisely so that the circuit configuration can be calibrated very exactly. One disadvantage of this solution, however, is the need for external reference resistors to be provided for each semiconductor chip situated on a circuit board, relative to which reference resistors the individual circuits of a semiconductor chip can be calibrated with different requirements. The configuration of external reference resistors situated outside a semiconductor chip, furthermore, has the disadvantage that the space on the system

circuit board is restricted and, consequently, an economic and cost-effective circuit board design can no longer be achieved.

A further possibility is to dispose the reference resistor within the semiconductor chip containing the circuit to be calibrated. Although such a configuration eliminates the problem of an increased space requirement on the circuit board, it, nonetheless, influences the accuracy of the reference resistance during operation because the latter is operated under the same ambient conditions as the semiconductor chip itself and is, thus, subject to the corresponding fluctuations.

The specification and setting of a reference resistor can only be effected in the production process. The reference resistor can be altered and set depending on manufacturing tolerances and device specifications in the manufacturing process by metal options, fuses, or other physical processes.

A circuit configuration that is calibrated relative to a reference resistor may be contained, for example, in an output driver stage of an off-chip driver, the calibration of the circuit configuration effecting a calibration of the output driver stage. Output driver or amplifier stages generally include complementary field-effect transistors. At least one transistor of an n-channel and a p-channel type are present,

which transistors are connected in series. A plurality of transistors of the same type may be connected in parallel with the p-channel and n-channel field-effect transistors. The resistor or the impedance is formed by at least one of the field-effect transistors of the output driver, the connection or disconnection of the respective parallel field-effect transistors enabling the desired resistance to be set. The reference resistor and the resistor of the output driver form a voltage divider in a series circuit. A partial voltage to be tapped off between the two resistors is fed to a comparator with another, fixedly defined voltage, which comparator compares the voltages fed to it. The resistor to be set is set by a control signal generated by the comparator until the two voltages fed to the comparator correspond to one another. The voltages may correspond to one another, for example, if the fixedly defined voltage and the partial voltage correspond to half the supply voltage of the voltage divider. The resistances of the two resistors also correspond to one another in this case.

The problem of a reference resistor subject to the operating fluctuations is manifested here: if such a reference resistor deviates from its desired resistance by 10%, then the voltage to be tapped off between the resistors will amount to half the supply voltage only when the resistor to be set likewise has a deviation of 10% of the desired resistance.

Summary of the Invention:

It is accordingly an object of the invention to provide a calibration configuration that overcomes the hereinafore-mentioned disadvantages of the heretofore-known devices of this general type and that is as simple as possible and in which a variable resistor is calibrated relative to a reference resistor so that a desired output impedance of the resistor to be set is achieved as exactly as possible.

With the foregoing and other objects in view, there is provided, in accordance with the invention, a calibration configuration, including a first voltage divider having a variable resistor and a resistor connected in series and defining a terminal therebetween for tapping off a partial voltage between the variable resistor and the resistor, a positive terminal connected to the variable resistor for feeding in a positive supply potential of a supply voltage, and a negative terminal connected to the resistor for feeding in a negative supply potential of the supply voltage. The calibration configuration has a circuit configuration with an output terminal for providing a voltage, a further resistor having a value in a fixed relationship with a resistance of the resistor of the first voltage divider, an evaluation device connected to the further resistor and generating a control signal dependent upon a value derived from the further

resistor, and a voltage generator connected to the evaluation device and generating the voltage from a multiplicity of possible voltages in a manner dependent on the control signal. The calibration configuration also has a comparator with a first input connected to the output terminal of the circuit configuration for feeding in the voltage, a second input connected to the terminal for tapping off the partial voltage, and an output terminal for outputting a comparison result of a comparison of the voltage and the partial voltage respectively fed in at the first input and at the second input. Also, the calibration configuration has a control logic unit connected downstream of the comparator with respect to an input-to-output direction of the comparator, the control logic unit having an output terminal coupled to the variable resistor of the first voltage divider and generating, dependent upon the comparison result, a control signal at the output terminal driving the variable resistor.

The calibration configuration has the advantage that, in order to calibrate the first variable resistor of the first voltage divider, a voltage is generated in a manner dependent on the resistance of the reference resistor so that the voltage fed to the comparator compensates for fluctuations in the resistance of the reference resistor and a desired output impedance of the resistor to be set is obtained as exactly as possible.

In accordance with another feature of the invention, the circuit configuration has an input terminal for feeding in a reference current and a terminal for tapping off a voltage across the further resistor, the terminal being connected to the input terminal and to the further resistor and a voltage dependent upon the reference current being tapped off at the terminal, and the evaluation device is connected to the terminal for tapping off the voltage across the further resistor and has an output terminal for tapping off the control signal therefrom.

In accordance with a further feature of the invention, the circuit configuration has a further resistor having a terminal at which a voltage can be tapped off in a manner dependent on the reference current.

In accordance with an added feature of the invention, the circuit configuration has a voltage generator with a multiplexer and a further voltage divider, the voltage generator is connected downstream of the evaluation device with respect to an input-to-output direction of the evaluation device, the multiplexer, dependent upon the control signal output by the evaluation device, selecting a voltage from a plurality of voltages provided by the further voltage divider

and providing the selected voltage as the voltage at the output terminal.

In accordance with an additional feature of the invention, the evaluation device has a combination element, which is connected to the further resistor through the terminal, and that the combination element takes up the voltage across the further resistor and has a further terminal for feeding in values representing the supply potentials of the supply voltage, a value representing the target impedance of the first resistor that is to be set, and a value representing the reference current.

In accordance with yet another feature of the invention, the evaluation device has an analog-to-digital converter, which is connected downstream of the combination element and which converts the output signal of the combination element into a control signal, for outputting at the output terminal of the evaluation device.

In accordance with yet a further feature of the invention, the combination element is programmed to carry out the calculation: / R * Icopy + Vrefcopy) where: Vrefcopy corresponds to the voltage across the further resistor; V corresponds to a supply voltage to be fed to the first voltage divider; R corresponds to the variable resistor of the first

voltage divider; and Icopy corresponds to the reference current of the circuit configuration.

In accordance with yet an added feature of the invention, the voltage divider includes a resistor network having a multiplicity of resistors, which, for their part, are connected in series. The voltage divider has at least one intermediate for tapping off a value of the voltage Vcomp.

In accordance with yet an additional feature of the invention, the multiplexer is driven by the output signal of the evaluation device and couples one of the intermediate taps of the voltage divider to the output terminal in a manner dependent on the output signal of the evaluation device.

In accordance with again another feature of the invention, the calibration configuration has an output driver having at least two field-effect transistors of complementary channel types, whose drain-source paths are connected in series, and that the first resistor of the first voltage divider is formed by at least one of the field-effect transistors of the output driver.

In accordance with again a further feature of the invention, at least one further field-effect transistor is in each case connected in parallel with the field-effect transistors and

the gate terminals of the field-effect transistors are connected to the output terminal of the control logic unit for the purpose of feeding the control signal and for the purpose of disconnecting or connecting the parallel field-effect transistors.

In accordance with again an added feature of the invention, the calibration configuration is monolithically integrated on an integrated semiconductor chip.

In accordance with a concomitant feature of the invention, the first voltage divider and the comparator are monolithically integrated in a semiconductor chip, and the evaluation unit is disposed in an automatic test machine not situated on the semiconductor chip, the automatic test machine serving for testing the semiconductor chip.

The calibration configuration according to the invention has the advantage that, in the event of fluctuations in the resistance of the reference resistor, a setting of the reference resistor in the manufacturing process, for example, allows a higher tolerance range with regard to the resistance. The calibration configuration enables the generation of a voltage Vcomp in a manner dependent on the reference resistor, which voltage is compared with the partial voltage to be tapped off at the reference resistor. Consequently, the

voltage Vcomp to be generated can be adapted to the voltage across the reference resistor so that a desired impedance of the variable resistor is obtained.

Furthermore, the calibration configuration according to the invention can be used to adapt a multiplicity of reference resistances without forming a setting of the reference resistor.

An exact setting of a reference resistor can be effected in the manufacturing process by, for example, metal options or fuses, but means a further process step for each individual semiconductor chip, thus affecting the production cost. Utilizing a first voltage Vcomp generated in a manner dependent on the actual resistance of the reference resistor in the calibration configuration makes it possible to compensate for the manufacturing tolerances of the reference resistor in a very simple and cost-effective manner.

Other features that are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a calibration configuration, it is, nevertheless, not intended to be limited to the details shown because various modifications and structural changes may be made

therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof, will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

FIG. 1 is a schematic circuit diagram of a prior art calibration configuration;

FIG. 2 is a schematic and block circuit diagram of a calibration configuration according to the invention;

FIG. 3 is a schematic and block circuit diagram of an exemplary embodiment of a circuit configuration according to the invention that generates the voltage;

FIG. 4 is a schematic and block circuit diagram of a voltage generator according to the invention; and

FIG. 5 is a schematic circuit diagram of an exemplary embodiment of an output driver according to the invention representing a variable resistance.

Description of the Preferred Embodiments:

Referring now to the figures of the drawings in detail and first, particularly to FIG. 2 thereof, there is shown a block diagram of the calibration configuration according to the invention. The calibration configuration 1 illustrated in FIG. 2 has a voltage divider with a first resistor R and a resistor Rref, which, for their part, are connected in series. A positive supply potential VDDQ is fed to one end of the series circuit at its terminal 15 and a negative supply potential VSSQ of a supply voltage is fed to the other end of the series circuit at the terminal 17. The series circuit has a terminal 16 at the node between the resistors R and Rref, at which terminal 16 a partial voltage Vref can be tapped off.

The calibration configuration 1, furthermore, has a circuit configuration 2, at the output terminal 11 of which a voltage Vcomp can be tapped off. A comparator 3 is connected, by a first input terminal 12, to the output terminal 11 of the circuit configuration 2 and, by a second input 13, to the tap 16 of the series circuit including the resistors R and Rref. The voltage Vcomp and the partial voltage Vref are fed to the comparator 3 through the first input 12 and through the second input 13, respectively. The comparator 3 compares the voltages present at its inputs 12 and 13 and outputs a signal 145 at an output terminal 14. A control logic unit 6, connected

downstream of the comparator 3, evaluates the control signal 145 generated by the comparator 3 and generates at the output terminal 18 a control signal 185 for driving and setting the first resistor R of the first voltage divider.

If the two voltages fed to the comparator correspond to one another, the setting of the resistor R by the control signal is concluded so that the resistor R has the desired impedance.

The circuit configuration 2 illustrated in FIG. 3 has a current path with an input terminal 21 for feeding in a reference current Icopy and a resistor Rrefcopy. The resistance of the resistor Rrefcopy is in a fixed relationship with the resistance of the resistor Rref of the first voltage divider illustrated in FIG. 2. The current path has a terminal 22, at which a voltage Vrefcopy can be tapped off in a manner dependent on the reference current Icopy. An evaluation device 9 includes a combination element 91 and an analog-to-digital converter 92 connected downstream. The combination element 91 is connected to the terminal 22 for tapping off the voltage Vrefcopy. Through a further terminal 23, the combination element 91 is fed values representing the supply potentials VDDQ, VSSQ of the supply voltage, a value representing the target impedance to be set of the first resistor of the first voltage divider, and a value representing the reference current Icopy. Based upon the signals present at its inputs 22

and 23, the combination element 91 generates an analog output signal 93, which is fed to the analog-to-digital converter 92. In such a case, the combination element 91 performs the following calculation to determine the control signal 93:

Proceeding from:

$$V = V_R + V_{Rref},$$

$$V_{Rref} = I * (R_{ref} + \Delta R_{ref}), \text{ and}$$

$$V_{copy} = I_{copy} * (R_{refcopy} + \Delta R_{ref})$$

where:

R corresponds to the first resistor of the first voltage divider;

R_{ref} corresponds to the resistor of the first voltage divider;

ΔR_{ref} corresponds to the deviation of the reference resistor from its desired resistance;

$R_{refcopy}$ corresponds to the resistor that is in a fixed relationship with the resistance of the first resistor R_{ref};

V corresponds to the supply voltage of the first voltage divider;

V_R corresponds to the voltage across the first resistor R;

V_{ref} corresponds to the voltage across the resistor R_{ref},

V_{copy} corresponds to the voltage across the resistor $R_{refcopy}$,

I corresponds to the current that flows through the first voltage divider; and

I_{copy} corresponds to the reference current that flows through the resistor $R_{refcopy}$,

the following results for the voltage V_{Rref}:

$$V_{ref} = (V_{copy} * V) / (R * I_{copy} + V_{copy}).$$

The voltage V_{ref} determined as a result thereof corresponds to the first voltage Vcomp generated at the output terminal 11 of the circuit configuration 2.

The analog-to-digital converter 92 converts the analog signal 93 into a digital signal 25 for outputting at the output terminal 24 of the evaluation device 9. A voltage generator 20

is connected downstream of the evaluation device 9. The voltage generator has a multiplexer 8 and a voltage divider 7.

In the preferred embodiment shown in FIG. 4, the voltage generator 20 shown in FIG. 3 includes a multiplexer 8 connected downstream of a voltage divider 7. The voltage divider 7 has a multiplicity of resistors 71, 72, 73 and 74 connected in series. The ends of the series circuit including the resistors of the voltage divider 7 are fed the positive supply potential VDDQ at the terminal 26 and the negative supply potential VSSQ of a supply voltage at the terminal 27. A multiplicity of possible voltages is generated from the supply voltage with the aid of the voltage divider 7. The number of resistors of the voltage divider 7 may be high so that a high number of different voltages can be generated on the signal lines 75, 76, 77. The resistors of the voltage divider 7 may be conventional non-reactive resistors or, else, resistors having complex elements. The resistors can also be realized by semiconductor components. The multiplexer 8 has terminals 81, 82 and 83, connected to the signal lines 75, 76 and 77, for tapping off the individual voltages of the voltage divider. In a manner dependent on a control signal generated by the evaluation device 9, the multiplexer 8 switches a connection to one of the terminals 81, 82 and 83 by the switch 84. One of the voltages generated by the resistor network is

present as voltage Vcomp at the output terminal 11 of the voltage generator 20.

As illustrated in FIG. 5 as an exemplary embodiment, the variable first resistor R of the first voltage divider shown in FIG. 2 is formed by one of the semiconductor components 41, 42, 411 and 421 of an output driver. In an output driver, a first p-channel field-effect transistor 41 and a first n-channel field-effect transistor 42 are connected in series with regard to their drain-source paths. The positive supply potential VDDQ of the supply voltage is fed to the source terminal of the field-effect transistor 41 through the terminal 15. At least in each case one further p-channel field-effect transistor 411 and n-channel field-effect transistor 421 are connected in parallel with the field-effect transistors 41 and 42. The resistor R is formed by at least one of the field-effect transistors 41, 42, 411, and 421 of the output driver. The gate terminals of the field-effect transistors 411 and 421 are connected to the output terminal 18 of the control logic unit 6 for feeding the control signal having n bits. A coding device (not shown here) in the semiconductor chip stores the information concerning how the field-effect transistors have to be controlled so that the desired impedance of the output driver is achieved. In each case only the n-channel field-effect transistor 421 or the p-channel field-effect transistor 411 is connected or

disconnected by the coding information upstream of the control logic unit 6 and the control signal 185 generated by the control logic unit 6 at the output terminal 18. The impedance of the output driver can be adapted, for example, in the time period of 100 milliseconds, because temperature fluctuations during operation of the semiconductor chip result in a change in the impedance of the output driver within this time period.